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EXAMINER	
ROBERTS, JESSICA M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,380	THANGARAJ ET AL.	
	Examiner	Art Unit	
	Jessica Roberts	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14, 16, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14, it is indefinite because it is not clear if the address is loaded into a register based from the least significant bit.

Claim 16 is indefinite because it is unclear if the address is loaded into a register based from the least significant bit. Claim 18 is indefinite because it is not clear if the address is load into a register based from the least significant bits, or just the ending address. As best understood by the examiner, the examiner takes the position that the address is loaded to an address based from the least significant bits.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Sugiyama et al., US-2003/00009722

Regarding claim 1, Malladi teaches A method for decoding video data, said method comprising: writing a starting address associated with the byte in a table (column 4 line 25-29 and fig. 4); and fetching data from the memory starting from the byte (column 15 line 39-41 and fig. 4). Malladi is silent in regards to writing a start code starting at a byte in a middle portion of a data word in a memory. However, Sugiyama teaches writing a start code starting at a byte in a middle portion of a data word in a memory ([0123] and fig. 13A and 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyamas' teachings of the start code starting in the middle the word to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 2, the combination of Malladi and Sugiyama as a whole teaches everything claimed as applied above (see claim 1). In addition, Malladi teaches wherein the start code is associated with a slice (Malladi, column 8 line 32-34).

Regarding claim 3, the combination of Malladi and Sugiyama as a whole teach everything claimed as applied above (see claim 1). Sugiyama further teaches wherein the data word comprises at least 16 bytes (Sugiyama, fig. 14). Therefore, it would have been obvious for one of ordinary skill I the art at the time of the invention to combine the

teaching of Malladi with Sugiyamas' teaching of a data word of at 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 4, the combination of Malladi and Sugiyama as a whole further teach writing another start code to another byte (Malladi teaches more than one start code, column 10 line 63-65) in a middle portion of another data word in the memory (Sugiyama, fig. 14); writing another address associated with the another byte in the table (Malladi, column 10 line 60-67); and wherein fetching data from the memory starting from the byte further comprises: fetching data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be obvious that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system checks for another start code (column 10 line 66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, the examiner notes that the byte at the end of the start code would be the byte preceding another start code.

Regarding claim 5, the combination of Malladi and Sugiyama as a whole further teaches looking up the address in the table (Malladi teaches writing to the start code table, column 4 line 25-29. The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 6, the combination of Malladi and Sugiyama as a whole further teaches where looking up the another address in the table (Malladi teaches writing to the start code table, column 4 line 25-29 The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 7, Malladi teaches system for decoding video data (abstract and column 1 line 24-26), said system comprising: a memory comprising a plurality of data words (Malladi, start code table, fig. 4), for storing a start code (fig. 4); a table for storing a starting address associated with the byte (Malladi, fig. 4); and a direct memory access module for providing data from the memory starting from the starting address (Malladi, column 21-24). Malladi is silent in regards to the start code starting at a byte in a middle portion of a particular one of the data words. However, Sugiyama teaches start code starting at a byte in a middle portion of a particular one of the data words, fig. 14. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyamas' teachings of the start code starting in the middle the word to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 8, the combination of Malladi and Sugiyama as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi teaches a video

transport processor (Malladi, fig. 4:417) for writing the start code starting at a byte in a middle portion of the particular data word in the memory (Sugiyama, fig. 14).

Regarding claim 9, the combination of Malladi and Sugiyama as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi wherein the start code is associated with a slice (Malladi, start code, column 8 line 32-34 and fig. 1A).

Regarding claim 10, Malladi and Sugiyama as a whole teaches everything claimed above (see claim 7). Malladi is silent in regards to the data word comprises at least 16 bytes.

However, Sugiyama teaches the data word comprises at least 16 bytes (Sugiyama, fig. 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Malladi with Sugiyamas' teaching of the data word comprising at least of 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 11, the combination of Malladi and Sugiyama as a whole further teaches wherein the video transport processor (Malladi, fig. 4:417) writes another start code (Malladi, teaches more than one start code, column 10 line 63-65) in the memory and wherein the table stores another address associated with the another byte in the table (Malladi, start code table, fig. 4) and wherein the direct memory access module

fetches data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be clear that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system checks for another start code (column 10 line 66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, it is clear that the byte at the end of the start code would be the byte preceding another start code). Malladi is silent in regards to another byte in a middle portion of another data word.

However, Sugiyama teaches another byte in a middle portion of another data word (Sugiyama, fig. 14)

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyamas' teaching of a start code in the middle of a data word to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 12, the combination of Malladi and Sugiyama as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi teaches a master processor for looking up the address in the table (Malladi, column 15 line 38-42).

Regarding claim 13, the combination of Malladi and Sugiyama as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi wherein the master processor looks up the another address in the table (Malladi, teaches writing more than one start code, column 10 line 60-67. The examiner notes, since Malladi writes more than one start code, and it polls the entire start code table, it is clear that more than one address is looked up, Malladi, column 15 lines 38-42).

Claim Rejections - 35 USC § 103

5. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Sugiyama et al., US- US-2003/00009722 and in further view of Son et al., US-5, 898,897.

Regarding claim 14, The system of claim 7, wherein the direct memory access module (Malladi, column 21-24) further comprises: a buffer comprising a plurality of data words for storing the video data from the starting address (Malladi, Malladi discloses where the parameters are loaded into a predefined memory location, column 7 line 63 to column 8 line 1-8. Further, Malladi discloses this process is done for multiple start codes, column 8 line 15-42); the first masking register (Malladi, column 3 line 65 to column 4 line 1-5); a first masking register (Malladi, column 3 line 65 to column 4 line 1-5). Malladi is silent in regards to a plurality of bytes corresponding to byte positions (Sugiyama, the slice start code contains the vertical position, [¶0110]. Further, Sugiyama discloses that each code boundary is byte assigned, and in the slice layer only the slice start code is byte assigned [¶0019]. The examiner notes that since each code word code is byte assigned, it would be obvious that the code words would include

the byte positions); a byte position that is less than the four least significant bits of the starting address are loaded with a first value and wherein each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is equal or greater than the four least significant bits of the starting address are load with a second value (Sugiyama, [¶0359]. Since Malladi discloses loading of parameters column 7 line 63 to column 8 line 1-8, and Sugiyama discloses the vertical position information ranges from [00 00 01 01] to [00 00 01 AF], the combination of Malladi and Sugiyama as a whole would be fully capable of loading a first and second address to a register or memory dependent upon the least significant bits). The combination of Malladi and Sugiyama as a whole are silent in regards to a first masking register for discarding a portion of a first data structure that precedes the starting address; a state machine for loading the first masking register. However, Son discloses a first masking register for discarding a portion of a first data structure that precedes the starting address (Son, column 8 line 53-56); a state machine (Son, fig. 3:307) for loading the first masking register with a pattern wherein each byte of the plurality of bytes in the first mask register (Son, column 10 line 30-40). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi and Sugiyama with the teachings of Son for providing detection of signal featur4es such as a start code in a bit stream that may be formatted in accordance with any of a plurality of formatting standards.

Regarding claim 15, the combination of Malladi, Sugiyama and Son as a whole teaches everything as claimed above (see claim 7). In addition Malladi teaches an

arithmetic logic unit for performing a logical AND operation between a first one of the plurality of data words in the buffer and the first masking register (Malladi, column 9 line 48-51. The examiner notes that an ALU has be able to perform both the logical operation of AND/OR on the chip level).

Regarding claim 16, the analysis and rejection made in claims 7-15 also apply here for common subject matter.

Regarding claim 17, the analysis and rejection made in claims 7-15 also apply here for common subject matter.

Regarding claim 18, Son teaches a second masking register (Son, register file, fig. 3:324) for discarding a portion of a second data structure that follows the ending address (abstract, and column 8 line 53-56), and a state machine (Son, fig. 3:307) for loading the second masking register with a pattern wherein each byte of the plurality of bytes in the second mask register (Son, column 10 line 30-40). Son is silent in regards to the second masking register comprising a plurality of bytes corresponding to byte positions.

However, Sugiyama teaches plurality of bytes corresponding to byte positions (Sugiyama, the slice start code contains the vertical position, [¶0110]. Further, Sugiyama discloses that each code boundary is byte assigned, and in the slice layer only the slice start code is byte assigned [¶0019]. The examiner notes that since each code word code is byte assigned, it would be obvious that the code words would include the byte positions); corresponds to a byte position that is less than or equal to the four least significant bits of the ending address are loaded with the second value, and

wherein each byte of the plurality of bytes in the second mask register that corresponds to a byte position that is greater than the four least significant bits of the ending address are loaded with the first value (Sugiyama, [¶0359]); Sugiyama discloses the vertical position information ranges from [00 00 01 01] to [00 00 01 AF]

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Son with Sugiyamas' teaching of the register comprising a plurality of bytes corresponding to byte position to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

The combination of Son and Sugiyama as a whole are silent in regards to loading of parameters.

However, Malladi discloses loading of parameters column 7 line 63 to column 8 line 1-8, the combination of Malladi and Sugiyama as a whole would be fully capable of loading a first and second address to a register or memory dependent upon the least significant bits. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Son and Sugiyama with the teachings of Malladi for providing a procedure for intelligently partitioning decoding task between software and hardware.

Examiner's Note

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant

to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sumida et al., US-7, 130,265 Data Multiplexing device and data multiplexing method, and data transmitter

Wise, et al., US- 6,799,246 Memory interface for reading/writing data from/to memory

Sullivan et al., US-2004/0030665 Methods and systems for preventing start code emulation at locations that include non-byte aligned and/or bit-shifted positions

Lee et al., US-5, 995, 707 Speed change reproduction recording apparatus for VCR of digital HDTV and method thereof

Chiba et al., US-2003/0058143 Image coding apparatus, variable length coding apparatus, control apparatus and method thereof

Sullivan et al., US-7, 248, 740 Method and system for preventing start code emulation at locations that include non-byte aligned and/or bit shifted positions

Balakrishnan et al., US-7, 227,899 Method and system for re-multiplexing of content modified MPEG-2 transport streams using interpolation of packet arrival times

Lempel et al., US-6, 178,203 Method and apparatus for two-row decoding of MPEG video

Bakhmutsky et al., US-5, 963,260 Macroblock level partitioned HDTV video decoder and related method

James et al., US-5, 495,592 System for finding and setting address portion of variable length character string by XORING portion in number of byt4es within single instruction

Dinkjian et al., US-5, 465,374 Processor for processing data strings by byte-by-byte

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jessica Roberts whose telephone number is (571) 270-1821. The examiner can normally be reached on 7:30-5:00 EST Monday-Friday, Alt Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JMR/

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